REPLACEMENT PARAGRAPH: Page 1, lines 11-15

This application is a divisional application serial no. [________] 09/835,115, **[Agents Docket Number ONX-115A,]** entitled "MEMS Mirrors With Precision Clamping Mechanism," filed April 12, 2001, which is based on and claims priority from Provisional Application 60/250,081 filed November 29, 2000.

Version with Markings to Show Changes Made

A1

This application is a divisional application serial no. 09/835,115, entitled "MEMS Mirrors With Precision Clamping Mechanism," filed April 12, 2001, which is based on and claims priority from Provisional Application 60/250,081 filed November 29, 2000.

REPLACEMENT PARAGRAPH: Page 5, lines 1-7.

A2

A first embodiment of the invention is shown in Fig. **2A**, which shows an apparatus **200A** having a movable flap that can be precisely clamped by electrodes on either 0 or 90 degrees surfaces. Such a structure allows the flap to be clamped, for example, in either a vertical or horizontal position. Such a flap may be used as part of an array of several MEMS mirrors in a planar matrix switch.

Version with Markings to Show Changes Made

A first embodiment of the invention is shown in Fig. **2A**, which shows an apparatus **[200]** **200A** having a movable flap that can be precisely clamped by electrodes on either 0 or 90 degrees surfaces. Such a structure allows the flap to be clamped, for example, in either a vertical or horizontal position. Such a flap may be used as part of an array of several MEMS mirrors in a planar matrix switch.

REPLACEMENT PARAGRAPH: Page 10, line 29 to page 11, line 25

A3

Figs. **4A-4H** depict an example of a process for fabricating a structure of the type shown in Fig. **2A**, Fig. **2B**, Fig. **3A** or Fig. **3B**. The structure is formed from a starting material wafer **400** having a device layer **403**, a substrate layer **401** and an insulator layer **402** disposed between the device and substrate layers as shown in Fig. **4A**. The base and/or device layer may be made of a crystalline material. For example, the starting material is typically a silicon-on-insulator (SOI) wafer with a silicon <110> handle substrate as the substrate layer **401**; the device layer can be standard silicon of <100> orientation; and the insulating layer can be an oxide formed, e.g., by oxidation of a surface of the substrate layer **401**. Alternatively, the starting material may be a silicon-on-nitride wafer or any other suitable type of wafer material known to the art. The device layer **403** may be used, for example to form a mirror plate for a MEMS optical switch, or an array of such switches, such as that shown in Fig. 6. In the first step Fig. 4B, two parallel deep trenches **404** that reach the buried oxide **402** may be formed in the substrate layer **401** from the backside of the wafer **400**. The widths of the trenches **404** may be sufficiently narrow that they can be completely filled-in during a later step. The trenches **404** may define the periphery of a cavity **415** that may be formed to accommodate a flap similar to those described above with respect to Figs 2-3B. It is also possible to form a single continuous trench that defines the periphery of the cavity. The trench or trenches **405** may be etched by an anisotropic etchant like KOH with silicon nitride or silicon oxide mask (not shown for simplicity). Alternatively, the trenches **404** may be formed in the substrate layer **401** prior to bonding the device layer **403** to the substrate layer **401**.

REPLACEMENT PARAGRAPH: Page 10, line 29 to page 11, line 25
Version with Markings to Show Changes Made

Figs. **4A-4H** depict an example of a process for fabricating a structure of the type shown in Fig. **2A**, Fig. **2B**, Fig. **3A** or Fig. **3B**. The structure is formed from a starting material wafer **400** having a device layer **403**, a substrate layer **401** and an insulator layer **402** disposed between the device and substrate layers as shown in Fig. **4A**. The base and/or device layer may be made of a crystalline material. For example, the starting material is typically a silicon-on-insulator (SOI) wafer with a silicon <110> handle substrate as the substrate layer **401**; the device layer can be standard silicon of <100> orientation; and the insulating layer can be an oxide formed, e.g., by oxidation of a surface of the substrate layer **401**. Alternatively, the starting material may be a silicon-on-nitride wafer or any other suitable type of wafer material known to the art. The device layer **403** may be used, for example to form a mirror plate for a MEMS optical switch, or an array of such switches, such as that shown in Fig. 6. In the first step Fig. 4B, two parallel deep trenches **404** that reach the buried oxide **402** may be formed in the substrate layer **401** from the backside of the wafer **400**. The widths of the trenches **404** may be sufficiently narrow that they can be completely filled-in during a later step. The trenches **404** may define the periphery of a cavity **415** that may be formed to accommodate a flap similar to those described above with respect to Figs 2-3B. It is also possible to form a single continuous trench that defines the periphery of the cavity. The trench or trenches **405** may be etched by an anisotropic etchant like KOH with silicon nitride or silicon oxide mask (not shown for simplicity). Alternatively, the trenches **[405]** <u>**404**</u> may be formed in the substrate layer **401** prior to bonding the device layer **403** to the substrate layer **401**.

REPLACEMENT PARAGRAPH: Page 12, line 27 to page 13, line 3.

Next, a hinged flap **410** may be formed from the top device layer **403** as shown in Fig. **4F**. The flap may optionally contain landing pads **408** on its bottom surface to minimize contact area with the base or sidewall and to provide electrical isolation as described above. The flap **410** may be mechanically connected to the base through a flexure or torsional beam similar to those depicted and described with respect to Fig. **2A**, allowing the flap **410** to move out of the plane of the base. A reflecting surface **413** may be formed on the surface of the flap **410** so that the resulting device may function as a mirror.

A4

Version with Markings to Show Changes Made

Next, a hinged flap **410** may be formed from the top device layer **403** as shown in Fig. **4F**. The flap may optionally contain landing pads **408** on its bottom surface to minimize contact area with the base or sidewall and to provide electrical isolation as described above. The flap **410** may be mechanically connected to the base through a flexure or torsional beam similar to those depicted and described with respect to Fig. **2A**, allowing the flap **410** to move out of the plane of the base. A reflecting surface **[410]** <u>**413**</u> may be formed on the surface of the flap **410** so that the resulting device may function as a mirror.